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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,695	07/24/2003	Kazuhiro Nakajima	8053-1016	9942

466 7590 07/31/2007

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EXAMINER	
NADAV, ORI	
ART UNIT	**PAPER NUMBER**
2811	

MAIL DATE	DELIVERY MODE
07/31/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/625,695	NAKAJIMA ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *31-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 31-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shea et al. (6,694,208) in view of Applicant Admitted Prior Art (AAPA).

Regarding claims 31, 39, 44 and 45, Shea et al. teach in related text (column 1, lines 20-25 and column 2, lines 57-65) a production process for producing plurality of a semiconductor devices on chip areas which are defined on a wafer, which production process comprises:

processing said wafer such that each of said chip areas is produced as a semi-finished semiconductor device by forming a first metal wiring layer on each of said chip areas;

subjecting said wafer to a provisional yield-rate test in which it is examined whether each of the semi-finished semiconductor devices on said wafer is acceptable or unacceptable; and

further processing said wafer such that each of said chip areas is produced as a finished semiconductor device when said wafer passes said provisional yield-rate test,

wherein a yield-rate of acceptable semi-finished semiconductor devices is found in said provisional yield-rate test, and it is determined that said wafer has passed said provision yield-rate test when said yield-rate exceeds a predetermined permissible rate. Shea et al. do not explicitly state that the further processing of said wafer include forming a second metal wiring layer on said first metal wiring layer.

AAPA teaches in figures 16 and 17 and related text (pages 1-5 and 35-38) further processing of said wafer includes forming a second metal wiring layer 48' on a first metal wiring layer 16'.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to further process said wafer of Shea et al. by forming a second metal wiring layer on said first metal wiring layer in order to obtain operational device by providing electrical connections to the device.

Regarding the claimed limitations of a yield-rate of acceptable semi-finished semiconductor devices is found in said provisional yield-rate test, and it is determined that said wafer has passed said provision yield-rate test when said yield-rate exceeds a predetermined permissible rate, these features are inherent in Shea et al.'s device, because Shea et al. teach a yield-rate of acceptable semi-finished semiconductor devices is found in said provisional yield-rate test, and then it determined that said wafer has passed said provision yield-rate test. The method for determining whether said wafer has passed said provision yield-rate test is done by counting the number of regions which failed and by dividing the number of defective chips by the total number

of chips (column 2, line 66 to column 3, line 21). This is synonymous to determining whether said yield-rate exceeds a permissible rate.

Regarding claims 31, 39 and 46, Shea et al. do not explicitly state forming a plurality of electrode test pads on an uppermost surface of said first metal wiring layer for carrying out a provisional yield rate test.

AAPA teaches in figures 16 and 17 and related text forming a plurality of electrode test pads 58', 88 on an uppermost surface of a metal wiring layer.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a plurality of electrode test pads on an uppermost surface of said first metal wiring layer for carrying out a provisional yield rate test in Shea et al.'s device in order to increase the reliability of the tests by using a well known conventional electrode pads.

Regarding claim 33, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form said customized wiring-arrangement section having a plurality of electrode pads formed on an uppermost surface of said second metal wiring layer, and wherein the electrode pads of said second metal wiring layer are arranged above the electrode pads of the first metal wiring layer with at least one insulating layer being intervened therebetween in prior art's device in order to increase the reliability of the tests by using a well known conventional electrode pads.

Regarding claims 34-35, Shea et al. teach subjecting said wafer to a genuine yield-rate test which it is examined whether each of the finished semiconductor devices on said wafer is acceptable or unacceptable thereby find a yield-rate of acceptable finished semiconductor devices; and finally processing said wafer when said wafer passes said genuine yield-rate test,

wherein a yield-rate of acceptable finished semiconductor devices is found in said genuine yield-rate test, and it is determined that said wafer has passed said genuine yield-rate test when said yield-rate exceeds a predetermined permissible rate.

Regarding claims 32, 36-37 and 40-42, AAPA teaches first metal wiring layer is formed as a basic wiring-arrangement section to define plural kinds of basic electronic component formation areas in each of said chip areas, and second metal wiring layer is formed as a customized wiring-arrangement section to establish electrical interconnections among said basic electrical component formation areas in accordance with a customer's request, wherein said basic wiring-arrangement section has a plurality of electrode pads 58' formed an uppermost surface thereof, for carrying out said provisional yield-rate test, wherein said basic wiring-arrangement section is formed as a multi-layered wiring-arrangement section 16' (see figure 16) composed at least two metal circuit pattern layers 36', 40' and at least one insulation layer 38' alternately laminated on each of said chip areas, and said customized wiring-arrangement section 48' is formed as a multi-layered wiring-arrangement section composed of at least two

metal circuit pattern layers and at least one insulation layer 54 alternately laminated on said basic wiring- arrangement section.

Therefore, prior art's device (that is, Shea et al.'s device modified by using AAPA's teachings) comprises a first metal wiring layer is formed as a basic wiring-arrangement section to define plural kinds of basic electronic component formation areas in each of said chip areas, and second metal wiring layer is formed as a customized wiring-arrangement section to establish electrical interconnections among said basic electrical component formation areas in accordance with a customer's request, wherein said basic wiring-arrangement section has a plurality of electrode pads formed an uppermost surface thereof, for carrying out said provisional yield-rate test, wherein said basic wiring-arrangement section is formed as a multi-layered wiring-arrangement section composed at least two metal circuit pattern layers and at least one insulation layer alternately laminated on each of said chip areas, and said customized wiring-arrangement section is formed as a multi-layered wiring-arrangement section composed of at least two metal circuit pattern layers and at least one insulation layer alternately laminated on said basic wiring- arrangement section.

Regarding claims 38 and 43, the electrode pads of said second metal wiring layer are vertically above the electrode pads of said first metal wiring layer, and the second test section is vertically above the first test section, in prior art's device, because the second metal wiring layer is located above the first metal wiring layer and the second test section is located above the first test section.

Regarding claims 39 and 44, Shea et al. teach first and second test sections (column 2, line 2-17 and 49-50).

Regarding claim 44, the claimed limitations of first and second test sections electrically connected to an active region of said chip area are inherent in prior art's device because the first and second test sections test the metal layers which in turn must be electrically connected to an active region of said chip area.

Claims 31-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maeda et al. (WO 01/63661) in view of Shea et al. (6,694,208).

Regarding claims 31, 39, 44 and 45, Maeda et al. teach in figures 20 and 21 and related text a production process for producing plurality of a semiconductor devices on chip areas which are defined on a wafer, which production process comprises:

processing said wafer such that each of said chip areas is produced as a semi-finished semiconductor device by forming a first metal wiring layer on each of said chip areas;

subjecting said wafer to a provisional test in which it is examined whether each of the semi-finished semiconductor devices on said wafer is acceptable or unacceptable; and

further processing said wafer such that each of said chip areas is produced as a finished semiconductor device when said wafer passes said provisional test,

further processing of said wafer to include forming a second metal wiring layer on said first metal wiring layer when said wafer passes said provisional test,

wherein an acceptable semi-finished semiconductor devices is found in said provisional test, and it is determined that said wafer has passed said provisional test.

Maeda et al. do not teach using yield-rate test such that said wafer has passed said provisional yield-rate test when said yield-rate exceeds a predetermined permissible rate.

Maeda et al. teach that any testing method can be used (page 36).

Shea et al. teach using yield-rate test such that said wafer has passed said provisional yield-rate test when said yield-rate exceeds a predetermined permissible rate (column 1, lines 20-25 and column 2, lines 57-65).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a yield-rate test in Maeda et al.'s device, such that said wafer has passed said provisional yield-rate test when said yield-rate exceeds a predetermined permissible rate in order to provide better quality product.

Regarding the claimed limitations of a yield-rate of acceptable semi-finished semiconductor devices is found in said provisional yield-rate test, and it is determined that said wafer has passed said provision yield-rate test when said yield-rate exceeds a predetermined permissible rate, these features are inherent in prior art's device, because Shea et al. teach a yield-rate of acceptable semi-finished semiconductor devices is found in said provisional yield-rate test, and then it determined that said wafer has passed said provision yield-rate test. The method for determining whether said

wafer has passed said provision yield-rate test is done by counting the number of regions which failed and by dividing the number of defective chips by the total number of chips (column 2, line 66 to column 3, line 21). This is synonymous to determining whether said yield-rate exceeds a permissible rate.

Regarding claims 31, 39 and 46, Maeda et al. teach forming a plurality of electrode test pads on an uppermost surface of a metal wiring layer.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a plurality of electrode test pads on an uppermost surface of said first metal wiring layer for carrying out a provisional yield rate test in Maeda et al.'s device in order to increase the reliability of the tests by using a well known conventional electrode pads.

Regarding claim 33, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form said customized wiring-arrangement section having a plurality of electrode pads formed on an uppermost surface of said second metal wiring layer, and wherein the electrode pads of said second metal wiring layer are arranged above the electrode pads of the first metal wiring layer with at least one insulating layer being intervened therebetween in prior art's device in order to increase the reliability of the tests by using a well known conventional electrode pads.

Regarding claims 34-35, prior art's device includes subjecting said wafer to a genuine yield-rate test which it is examined whether each of the finished semiconductor devices on said wafer is acceptable or unacceptable thereby find a yield-rate of acceptable finished semiconductor devices; and finally processing said wafer when said wafer passes said genuine yield-rate test,

wherein a yield-rate of acceptable finished semiconductor devices is found in said genuine yield-rate test, and it is determined that said wafer has passed said genuine yield-rate test when said yield-rate exceeds a predetermined permissible rate.

Regarding claims 32, 36-37 and 40-42, prior art's device includes first metal wiring layer is formed as a basic wiring-arrangement section to define plural kinds of basic electronic component formation areas in each of said chip areas, and second metal wiring layer is formed as a customized wiring-arrangement section to establish electrical interconnections among said basic electrical component formation areas in accordance with a customer's request, wherein said basic wiring-arrangement section has a plurality of electrode pads formed an uppermost surface thereof, for carrying out said provisional yield-rate test, wherein said basic wiring-arrangement section is formed as a multi-layered wiring-arrangement section (see figure 7 of Maeda et al.) composed at least two metal circuit pattern layers and at least one insulation layer alternately laminated on each of said chip areas, and said customized wiring-arrangement section is formed as a multi-layered wiring-arrangement section composed of at least two metal circuit pattern

layers and at least one insulation layer alternately laminated on said basic wiring-arrangement section.

Regarding claims 38 and 43, the electrode pads of said second metal wiring layer are vertically above the electrode pads of said first metal wiring layer, and the second test section is vertically above the first test section, in prior art's device, because the second metal wiring layer is located above the first metal wiring layer and the second test section is located above the first test section.

Regarding claims 39 and 44, Shea et al. teach first and second test sections (column 2, line 2-17 and 49-50). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use first and second test sections in prior art's device in order to improve the testing capabilities of the device.

Regarding claim 44, the claimed limitations of first and second test sections electrically connected to an active region of said chip area are inherent in prior art's device because the first and second test sections test the metal layers which in turn must be electrically connected to an active region of said chip area.

Response to Arguments

. Applicant argues that the test circuitry of Shea et al. is used to test a finished wafer, and Shea et al. do not disclose a provisional yield rate test on a semi-finished wafer.

Shea et al. explicitly state in column 1, lines 24-25 that tests are conducted during and after the manufacturing process. Therefore, Shea et al. teach a provisional yield rate test on a semi-finished wafer, as claimed.

The rest of applicant's arguments with respect to claims 31-46 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-4670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
7/24/07

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